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Implementation of Grid-Connected Cascaded Multi-Level Inverter Based on FPGA for Centralized Photovoltaic Generation[1]

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Abstract

This paper proposes a grid-connected cascaded multi-level inverter used in centralized photovoltaic generation. Field programmable gate array (FPGA) is applied to implement the multichannel Carrier Phase Shifting Sinusoidal Pulse Width Modulation(CPS-SPWM) strategy for the inverter. Analysis and practical implementation of the regular sampled three-phase CPS-SPWM waveform has been presented in this paper. An ALRERA FPGA chip is employed to fulfill all the function of modules, such as divider module, triangular carrier generation module, sine wave generation module, comparing module, dead time module and so on. The simulation and experimental results show that the presentation of this grid-connected cascaded multi-level inverter used in the photovoltaic generation system is feasible.

Keywords: photovoltaic generation; FPGA; cascaded multi-level inverter; CPS-SPWM

1.Introduction

As people are more and more concerned with the fossil fuel exhaustion and the environmental problems caused by the conventional power generation, renewable energy sources such as solar energy, wind power are wildly used. Photovoltaic system is one of important methods of utilizing solar energy. It has been used today in many applications such as lamp lighting, satellite power systems, home power supply etc[1]. Large-scale centralized solar grid-connected generating plant is an important form of photovoltaic generation. In the 21st century, many MW-level photovoltaic generating plants are coming

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forth in the world and higher scale can be expected. So the large-scale centralized solar grid-connected generating plant is a main direction of photovoltaic generation.

As the grid-connected photovoltaic inverter is one of the necessary equipment of the grid-connected photovoltaic system. Its design is very important for using the solar energy effectively and safely. The cascaded multi-level inverter has been widely used in high voltage fields. It has the advantages of good output waveform, low switching stress. Its structure is suitable for modularization. It is a kind of suitable choice of replacing the existing PWM inverter[2].

The multi-level has entered a new stage of development, there have been a variety of topologies which can be summed up in three kinds that divided into the following ways: diode-clamped structure, and capacitor-clamped structure and H-bridge cascade structure[3]. Compare with other two structures, the cascaded inverter needs the least components when the power level is the same that it is easy to implement redundant module with simple control, and can be mixed to achieve a combined application of a variety of devices that it is most viable under high-voltage output.

In this paper, a grid-connected cascaded multi-level inverter is proposed to apply to the large-scale photovoltaic generation. Based on the regular sampled three-phase CPS-SPWM strategy, H-bridge multi-level inverter has been constructed. Considering the large number of drive signals of PWM, FPGA is used in this inverter. Only An ALRERA FPGA chip can fulfill all the function of modules, such as divider module, triangular carrier generation module, sine wave generation module, comparing module, dead time module and so on. The simulation and experimental results show that the performance of this grid-connected cascaded multi-level inverter used in the photovoltaic generation system is feasible.

2.Photovoltaic Generation System Configuration

The photovoltaic generation system structure is shown in Fig.1. It employs two stages to appropriately condition the available solar power for feeding into the grid. The first stage comprises of a boost or buck-boost type DC/DC power converter topology is used to boost the photovoltaic (PV) array voltage and track the maximum solar power, in which the maximum power point tracking(MPPT) is implemented. The second stage use DC/AC power converter, which inverts this dc power into high quality ac power fed into the grid[4]. The inverter used in the second stage is a cascaded multi-level inverter, whose output is controlled so as to generate a fundamental real power injecting into the utility. Both stages are controlled by the floating-point DSP(digital signal processor) TMS320C2812 and FPGA Altera EP1k50QC208-3. The floating-point DSP TMS320C2812 has the powerful 32-bit floating-point calculation ability and the high integration of peripheral circuits used in converter control. FPGA serves as a coprocessor, producing all independent PWM pulses driving power converter.

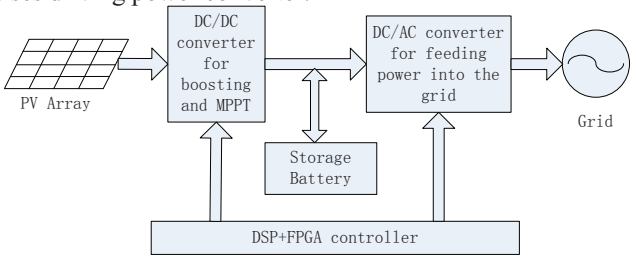

Figure 1. Grid-connected photovoltaic generation system structrue

3.Topology of Csacaded Multi-Level Inverter

A grid-connected cascaded multi-level inverter is proposed to apply to the large-scale photovoltaic generation. Fig.2 shows the topology of seven-level inverter. Every phase consists of three units which are

two-level H-bridge inverters with the same parameters. The output phase voltage is connected by three units in series. This seven-level cascaded inverter can output high quality sine wave. Since the high output voltage can be obtained, the cascaded multi-level inverter can connect with the grid directly without any transformer[5].

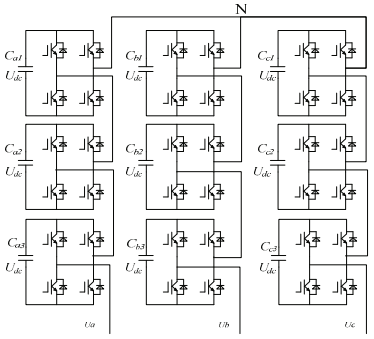

Figure 2. Cascaded 7-level inverter topology

4.Principle of Cps-Spwm

CPS-SPWM is one of switch modulated strategies fitting to high power electronic equipments. It is a PWM modulation which is specially for the combination converters and multi-level converters[6]. CPS-SPWM strategy can realize SPWM in high power occasion, improve waveform maximally, decrease output harmonic and capacity of filter and reduce the cost. Furthermore this technique can import all kinds of advanced control strategies and optimize whole system performance parameters because of its high equivalent switch frequency and wide transmission bandwidth. The basic principle of CPS-SPWM is: in the cascaded inverter with the cascaded unit number N, each inverter unit takes the common sinusoidal reference signal $u_s(\omega_s t)$, whose frequency is ω_s. The triangular carrier frequency of inverter unit is $k_c \times \omega_s$. Where k_c is the ratio of the triangular carrier frequency and the reference signal frequency .Each bridge's carrier is phase shifted by $1/(2N)$ of the triangular carrier period, and the phase of the L-th inverter unit is $\varphi_L = \varphi_c + \pi L/N$ (where φ_c is the phase of the triangular carrier. Then the output of the inverter with $2N+1$ level is born[7].

Fig.3 is the CPS-SPWM technology scheme for the A-phase cascaded inverter. $u_s(t)$ is the modulation signal, while the $c_i(t)(i=1,2,3)$ is the triangular carrier for each inverter unit. $u_{ai}(i=1,2,3)$ is the output voltage of each inverter unit, and u_a is the output phase voltage. Based on the theory of CPS-SPWM, the A-phase output is a seven-level waveform. By shifting an appropriate phase angle($2\pi/3$ for B-phase and $4\pi/3$ for C-phase) of modulation signal, both B-phase and C-phase can also get their outputs with the same method as A-phase.

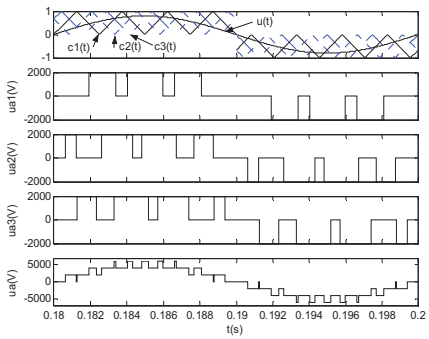

Figure 3. The scheme of CPS-SPWM

5.Implemeantation of Cps-Spwm Based on Fpga

FPGA belongs to the wide family of programmable logic components. Their densities are now exceeding 10 million gates. FPGA can be defined as a matrix of configuration logic blocks (combinational and/or sequential), linked to each other's by an interconnection network that is also entirely reprogrammable. Memory cells control the logic blocks as well as the connections so that the component can fulfill the required application specifications[8]. This provides flexibility to modify the designed circuit without altering the hardware part. Concurrent operation, less hardware, easy and fast circuit modification, comparatively low cost for a complex circuitry and rapid prototyping make it as the most favourable choice for prototyping an ASIC.

According to previous analyses of CPS-SPWM, logic circuits can be designed. The whole CPS-SPWM IC is divided five parts: divider module, triangular carrier generation module, sine wave generation module, comparing module and dead time module, as shown in Fig.4. Each module is programmed with Verilog HDL and compiled and simulated in the environment of Altera Quartus II. *M* is the modulation
ratio which is from DSP.

In Fig.4, the phase A~C outputs are the driving signals which are used to switch the power IGBTs. The configuration shown as Fig.4 is CPS-SPWM modulation system for three-phase cascaded inverter. Each phase output contains 3 inverter units with 6 driving signals desired. So FPGA can output 18 driving signals for 9 inverter units. Furthermore, a higher voltage output will be achieved by increasing cascaded unit number *N* and regulating the phase of triangular carriers at the same time.

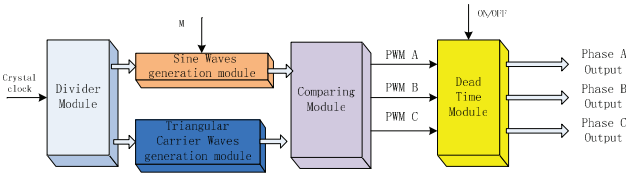

Figure.4 The system configuration of CPS-SPWM based on FPGA

In the following all the module are described in detail.

5.1.Divider Module

In order to get different clock signals of different frequency for each module, a divider is needed. It can generate the frequency which is 1/*n* of the basic clock. It is realized by programming. Fig.5 illustrates the scheme.

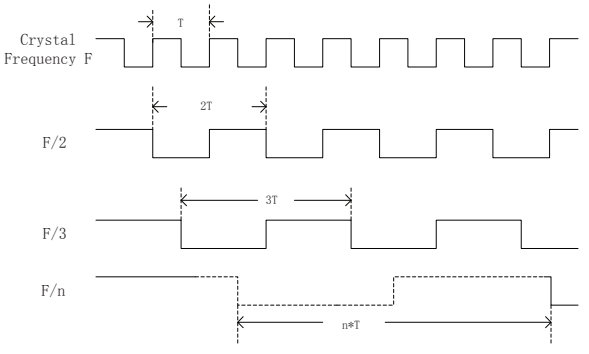

Figure 5 The scheme of divider module

5.2.Sine Wave Generation Module

Sinusoidal modulating waves are commonly used in PWM schemes, although other types of modulating wave, such as trapezoidal or triangular waves have been employed in certain applications. An alternative approach of sine wave generation is that to store the sine values in a lookup table, which is pre-programmed into permanent memory (PROM). The memory requirement, efficiency of operation, and accuracy of the output waveform depends on the number of sample values defining a cycle of the sine wave and their resolution. A modulating wave could be defined at a greater number of sample points, but the memory requirement is proportionally increased. Hence, the point at which a sample is taken for the modulating process directly corresponds to a value in the lookup table. If a single-phase carrier is generated the each frequency ratio must be a multiple of three to eliminate the carrier frequency harmonics[9].

5.3.Triangular Carrier Generation Module

The triangular carrier wave can be generated using software up/down counter. The rate at which this counter is incremented (or decremented) determines the carrier frequency and accuracy of the sampling process. Each time the counter is incremented (or decremented) its output is compared with a sampled value of the sinusoidal modulating wave to determine the switching edge of the PWM waveform. The sinusoidal modulating wave and triangular carrier wave are shown in Fig.6.

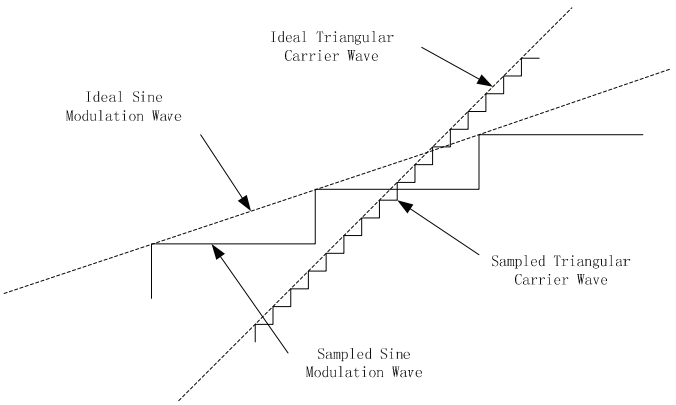

Figure 6 Illuatration of sampled process

5.4.Comparing Module

The comparing module outputs the CPS-SPWM waveforms after calculating the value of the digital carrier wave and modulation wave. It is achieved easily using programming. The principle of comparing is as follows. In each sampled period, if the value of u_s is greater than that of c_i(i=1,2,3), the driving signal of the i-th unit is set to “1” which represents turn-on. Otherwise it is set to “0” which represents turn-off.

5.5.Dead Time Module

The semiconductors devices used as power switches are not ideal, so they react with a certain delay to the driving signals corresponding to turn-on and turn-off. To avoid short-circuit in any leg of the power

inverter, dead time must be considered. It is performed by an independent counter, through which the rising edge of each output is delayed in a setting time. Fig.7 shows the generation of dead time.

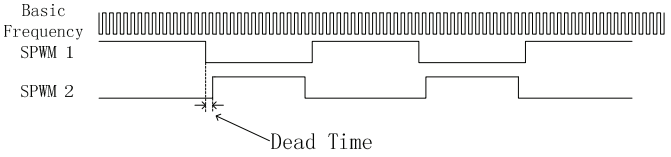

Figure 7 The generation of dead time

6.Simulation Results

The CPS-SPWM waveforms for a cascaded 7-level inverter are simulated using Quartus II. The proposed CPS-SPWM scheme is implemented on an ALRERA EP1K50QC208-3 FPGA, whose crystal frequency is 20MHz. Some simulation results have been chosen to illustrate some of the main features of CPS-SPWM waveforms generated by FPGA. Fig.8 shows the output of single-phase CPS-SPWM waveforms for 12 switches of cascaded inverter.Out1,2 are for the first unit,out3,4 are for the second unit, and out5,6 are for the third unit. The expanding view is shown as Fig.9 in which the dead time is obviously shown.

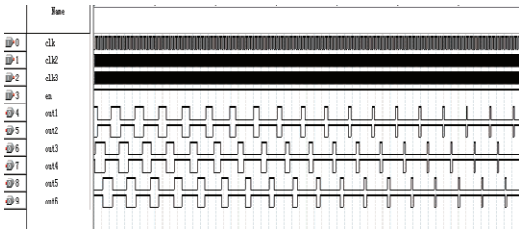

Figure 8 The output of single-phase CPS-SPWM waveforms

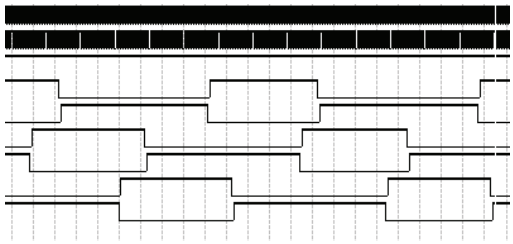

Figure 9 The expanding view of the output waveform

7.Experimaental Results

A prototype of single-phase grid-connected cascaded 5-level inverter has been developed using above described scheme and tested in the laboratory. Experimental results have been chosen to show the effectiveness of the proposed configuration. The voltage of grid is 220V, 50Hz. The DC source voltage of each unit is 140V.MOSFET is chosen for the power devices. The triangular carrier frequency is 2KHz.

Fig.10 is the waveform of a half cycle of SPWM. Fig.11 is the dead time of SPWM waveform. The output voltage of 5-level cascaded inverter is shown in Fig.12.

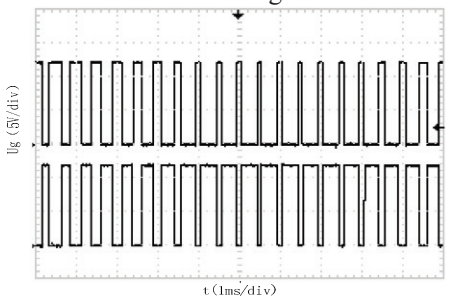

Figure 10 A half cycle of SPWM waveform

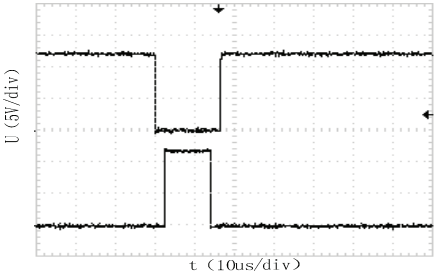

Figure 11 The dead time waveform

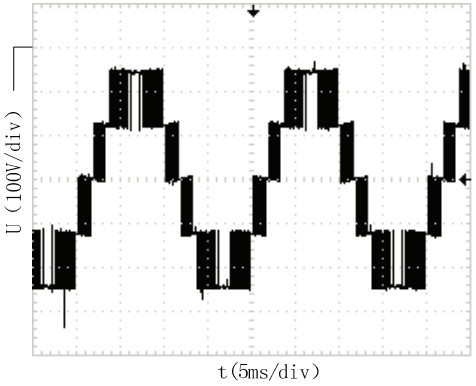

Figure 12 The output waveform of five-level inverter

8.Conclusion

In this paper the design and implementation of a three-phase cascaded multi-level inverter applied to the large-scale centralized solar grid-connected inverter is presented. All CPS-SPWM functions are realized within a single FPGA chip. Its redundancy can be easily realized by increasing the cascaded unit number. The simulation and experimental results are also provided to verify that the proposed scheme is feasible.

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